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EXAMINER	
RILEY, MARCUS T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,784	MURAKAMI, NAOYA	
	Examiner	Art Unit	
	Marcus T. Riley	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/3/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *attached*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 2** is objected to because of the following informalities:

Regarding claim 2; claim 2 states in part *"and an continuously"*. The word *"an"* appears to be a typographical error. It is assumed for continued examination purposes that the *"an"* is deleted.

Appropriate correction is required.

2. The following is a quotation of 37 CFR 1.75(a):

> The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

3. **Claim 5** is objected to under 37 CFR 1.75(a), as failing to particularly point out and distinctly claim the subject matter which application regards as his invention or discovery.

Regarding claim 5; claim 5 states in part *"the correction circuit executes the shading correction by sharing either of the monochromatic image signal and the color image signal."* It is not understood what is meant by the use of the word *"either"* followed further by the word *"and"*. Suggest changing the word *"and"* to the word *"or"*. Thus, it should read as follows... *"the correction circuit executes the shading correction by sharing either of the monochromatic image signal or the color image signal."*

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US 5,550,638, hereinafter Ikeda '638) in combination with Sakai et al. (US 5,784,180, hereinafter Sakai 180).

Ikeda '638 discloses an image reading apparatus comprising: a four line CCD sensor to receive a light reflected by a reading object and output either or both of a monochromatic image signal and a color image signal of R, G, and B {("*First, third, and fifth sensors (or CCDs) (58a, 60a, and 62a) are arranged on a line LA, and second and fourth sensors are arranged on a line LB separated from the line LA by four lines (63.5 .mu.m.times.4=254 .mu.m).*" column 7, lines 62-66) and see also ("*Registers 105d to 107d, and 108d to 110d are used to form a monochromatic image. An output can be obtained by performing weighting addition of colors by MONO=k.sub.1 Yi+l.sub.1 Mi+m.sub.1 Ci.*" column 15, lines 60-63)}; a correction circuit to execute shading correction for the monochromatic image signal ("*When AHi 148="1", image data sent from an external apparatus is synthesized; when BHi 123="1", color conversion is performed, as described above; and when DHi 122="1", monochromatic image data is calculated and output from the color correction circuit.*" column 41, lines 64-67 and column 42, line 1); where the correction circuit switches a correction operation of executing the shading correction for either or both of the monochromatic image signal and the color image signal of R, G, and B according to an image reading mode for the reading object or a reading state ("*...in FIG. 2, the switching signals are supplied through signal lines BHi 123, DHi 122, FHi 121, GHi 119, PHi 145, and AHi 148 as ON/OFF switching signals for the color conversion circuit B, the*

color correction circuit D, the character synthesizing circuit F, the image process and edit circuit G, the color balance circuit P, and the external apparatus image synthesizing circuit 502." column 38, lines 40-46).

Ikeda '638 does not expressly disclose a correction circuit to execute shading correction for the color image signal.

Sakai '180 discloses a correction circuit to execute shading correction for the color image signal. (*The R,G, and B digital signals are corrected by the shading correction circuit 3028 in the main scan direction. In addition, a pixel shift in the main scan direction is performed by the pixel shift correction circuit 3029."* column 22, lines 36-40).

They are combinable because they are from the same field of endeavor of an "Image Processing Apparatus" (*"It is still another object of the present invention to provide an image processing apparatus capable of storing a color image signal with high quality.* Sakai '180 at column 1, lines 56-58).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the image processing apparatus as taught by Ikeda '638 by adding a correction circuit to execute shading correction for the color image signal as taught by Sakai '180.

The motivation for doing so would have been because it would make available an image processing apparatus capable of storing a color image signal with high quality ("*It is still another object of the present invention to provide an image processing apparatus capable of storing a color image signal with high quality.*" Sakai '180 at column 1, lines 56-58).

Therefore it would have been obvious to combine Ikeda '638 with Sakai '180 to obtain the invention a specified in claim 1.

Regarding claim 2; Ikeda '638 discloses where the image reading mode includes at least one mode of a reading of the monochromatic image from the reading object, a reading of the color image from the reading object, an automatically selecting and reading either or both of the monochromatic image and the color image from the reading object, and an continuously and automatically reading either or both of monochromatic images and color images from a plurality of the reading objects (*"Color switching signals C.sub.0 ', C.sub.1 ', and C.sub.2 ' 366 to 368.are set by an output port 501 connected to the CPU bus 22, and the signal MAREA 364 is output from the area signal generation circuit J. Gate circuits 150d to 153d control so that when DHi="1" based on the non-rectangular area signal DHi 22 read out from a binary memory (bit map memory) L537, signals C.sub.0 ', C.sub.1 ', C.sub.2 '="1, 1, 0", thereby automatically outputting data for a monochromatic image."* column 16, lines 4-11).

Regarding claim 3; Ikeda '638 discloses where the reading state includes at least one of the time of turning on power, the start time of the image reading, the time of continuously reading the reading objects but before starting reading each of the reading objects, the time of automatically switching reading of the monochromatic image or the color image, and the time of adjustment mode (*"The memory corresponds to the 100-dpi memory L in the entire circuit shown in FIG. 2, and is used as a means for generating switching signals for determining an ON (executing) or OFF (not executing) state of various image process and edit modes, such as the above-mentioned color conversion, image trimming (non-rectangular trimming), image painting (non-rectangular painting), and the like for shapes illustrated in, e.g., FIG. 37E. More*

specifically,in FIG. 2, the switching signals are supplied through signal lines BHi 123, DHi 122, FHi 121, GHi 119, PHi 145, and AHi 148 as ON/OFF switching signals for the color conversion circuit B, the color correction circuit D, the character synthesizing circuit F, the image process and edit circuit G, the color balance circuit P, and the external apparatus image synthesizing circuit 502." column 38, lines 32-46).

Regarding claim 4; Ikeda '638 discloses where the four line CCD sensor is of a type of outputting the monochromatic image signal and the color image signal at the same time and there are a plurality of the correction circuits and each of the correction circuits executes the shading correction for the monochromatic image signal and the color image signal of R, G, and B (*"In this embodiment, since an original is read by the five staggered sensors which have an interval of four lines (63.5 .mu.m.times.4=254 .mu.m) in a sub scan direction, ...the preceding second and fourth channels and the remaining first, third, and fifth channels have a positional aberration. In order to normally connect outputs of these channels, the positional aberration correction circuit 504a comprising a memory of a plurality of lines corrects the positional aberration."* column 8, lines 64-67 thru column 9, lines 1-6)

Regarding claim 6; Ikeda '638 discloses where the correction circuit, in a reading mode to read the monochromatic image, switches to an operation of executing the shading correction for the monochromatic image signal outputted from the four line CCD sensor and not executing the shading correction for the color image signal (*"When a monochromatic signal described in the masking unit is selected, or when a three-color mode for forming an image using only Y, M, and C toners is selected, input image processing by the image area separation processing of this embodiment is not performed."* column 27, lines 10-14).

Regarding claim 7; Ikeda '638 discloses where the correction circuit, in a reading mode to read the color image, switches to an operation of not executing the shading correction for the monochromatic image signal outputted from the four line CCD sensor and executing the shading correction for the color image signal ("*When a monochromatic signal described in the masking unit is selected, or when a three-color mode for forming an image using only Y, M, and C toners is selected, input image processing by the image area separation processing of this embodiment is not performed.*" column 27, lines 10-14).

Regarding claim 8; Ikeda '638 discloses where the correction circuit, in a mode of automatically selecting and reading either or both of the monochromatic image and the color image, switches to an operation of executing the shading correction for both the monochromatic image signal and the color image signal outputted from the four line CCD sensor (*"Color selection is controlled by the CPU 20 in accordance with an output order to a color printer and the truth table shown in FIG. 12B based on (C.sub.0, C.sub.1, C.sub.2). Registers 105d to 107d, and 108d to 110d are used to form a monochromatic image. An output can be obtained by performing weighting addition of colors by MONO=k.sub.1 Yi+l.sub.1 Mi+m.sub.1 Ci."* column 15, lines 58-63).

Regarding claim 9; Ikeda '638 discloses where the correction circuit, in a mode of continuously reading a plurality of the reading objects, switches to an operation of executing the shading correction on the white level for the color image signal outputted from the four line CCD sensor. (*"When the CCD's (500a) for reading an original are located at a reading position of the uniform white plate (home position) in a color correction mode, an exposure lamp (not shown) is turned on, and image data of a uniform white level is stored in a one-line correction*

RAM 78a' prior to a copying operation or a reading operation. For example, if the main scan width corresponds to a width in a longitudinal direction of an A4 size, 16.times.297 mm=4,752 pixels for 16 pels/mm, that is, the capacity of the RAM is at least 4,762 bytes, and data of the white plate in units of pixels are stored in the RAM 78a', as shown in FIG. 6C, when white plate data Wi of an ith pixel (i=1 to 4,752) is as shown in FIG. 6B showing the principle of white correction." column 9, lines 63-67 thru column 10, lines 1-8).

6. **Regarding claim 5;** Ikeda '638 as modified does not expressly disclose a where the four line CCD sensor is of a type of independently outputting the monochromatic image signal and the color image signal and the correction circuit executes the shading correction by sharing either of the monochromatic image signal or the color image signal.

Sakai '180 discloses where the four line CCD sensor is of a type of independently outputting the monochromatic image signal and the color image signal and the correction circuit executes the shading correction by sharing either of the monochromatic image signal and the color image signal (*"An analog circuit 3025 amplifies analog outputs from the CCD line sensors 3061, 3062, and 3063 and converts these analog signals into digital signals. A generator 3026 for signal for adjustment generates a reference signal for the analog circuit 3025. A dark correction circuit 3027 performs dark correction of R, G, and B digital image signals from the analog circuit 3025. A shading correction circuit 3028 performs shading correction of an output signal from the dark correction circuit 3027. A pixel shift correction circuit 3029 corrects a main-scan pixel shift of an output signal from the shading correction circuit 3028."* column 21, lines 16-26).

They are combinable because they are from the same field of endeavor of an "Image Processing Apparatus" (*"It is still another object of the present invention to provide an image processing apparatus capable of storing a color image signal with high quality.* Sakai '180 at column 1, lines 56-58).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the image processing apparatus as taught by Ikeda '638 by adding correction circuit that executes the shading correction by sharing either of the monochromatic image signal or the color image signal as taught by Sakai '180.

The motivation for doing so would have been because it would make an image memory apparatus capable of reproducing a high-quality image as needed (*"It is an object of the present invention to provide an image memory apparatus capable of reproducing a high-quality image as needed..."* Sakai '180 at column 1, lines 39-41).

Therefore it would have been obvious to combine Ikeda '638 with Sakai '180 to obtain the invention a specified in claim 1.

7. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai '180 in combination with Ikeda '638.

Regarding claim 10; Sakai '180 discloses an image forming apparatus comprising: a correction circuit, according to an image reading mode for the reading object or a reading state, switches an operation of executing a shading correction for either or both of the monochromatic image signal and the color image signal of R, G, and B outputted from the four line CCD sensor

(*"The dark signal levels of the R, G, and B digital signals output from the analog circuit 3025 are corrected by the dark processing circuit 3027. The R, G, and B digital signals are corrected by the shading correction circuit 3028 in the main scan direction. In addition, a pixel shift in the main scan direction is performed by the pixel shift correction circuit 3029. For example, this correction is performed by shifting the write timings of the FIFO (First-In First-Out)."* column 22, lines 34-41); an image forming unit to form an image on the basis of either or both of the monochromatic image signal and the color image signal for which the shading correction is executed by switching the operation of the correction circuit (*"A dark correction circuit 3027 performs dark correction of R, G, and B digital image signals from the analog circuit 3025. A shading correction circuit 3028 performs shading correction of an output signal from the dark correction circuit 3027. A pixel shift correction circuit 3029 corrects a main-scan pixel shift of an output signal from the shading correction circuit 3028."* column 21, lines 20-26).

Sakai '180 does not expressly disclose a four line CCD sensor to receive a light reflected by a reading object and outputting either or both of a monochromatic image signal and a color image signal of R, G, and B.

Ikeda '638 discloses a four line CCD sensor to receive a light reflected by a reading object and outputting either or both of a monochromatic image signal and a color image signal of R, G, and B (*"First, third, and fifth sensors (or CCDs) (58a, 60a, and 62a) are arranged on a line LA, and second and fourth sensors are arranged on a line LB separated from the line LA by four lines (63.5 .mu.m.times.4=254 .mu.m)."* column 7, lines 62-66) and see also (*"Registers 105d to 107d, and 108d to 110d are used to form a monochromatic image. An output can be*

obtained by performing weighting addition of colors by MONO=k.sub.1 Yi+l.sub.1 Mi+m.sub.1 Ci." column 15, lines 60-63)

They are combinable because they are from the same field of endeavor of an "Image Processing Apparatus" (*"The present invention relates to an image processing apparatus which executes various processing operations of an input image to perform image edit operations.* Ikeda '638 at column 1, lines 13-15).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the image processing apparatus as taught by Sakai '180 by adding a four line CCD sensor to receive a light reflected by a reading object and outputting either or both of a monochromatic image signal and a color image signal of R, G, and B as taught by Ikeda '638.

The motivation for doing so would have been because it would *provide a simple, inexpensive image processing apparatus* (*"It is still another object of the present invention to provide a simple, inexpensive image processing apparatus."* Ikeda '638 at column 2, lines 39-40).

Therefore it would have been obvious to combine Sakai '180 with Ikeda '638 to obtain the invention a specified in claim 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marcus T. Riley whose telephone number is 571-270-1581. The examiner can normally be reached on Monday - Friday, 7:30-5:00, est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler Lamb can be reached on 571-272-7406. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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June 05, 2007

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